AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Currently Amended) An electrostatic discharge (ESD) protection circuit with low input capacitance, suitable for an I/O pad, comprising:

a first power line;

a second power line; and

a plurality of diodes, stacked and coupled between the first power line and the I/O pad, wherein during normal operation, the diodes are reverse-biased, and, when an ESD event occurs between the second power line and the I/O pad, the diodes are forward-biased to conduct ESD current;

~~The ESD protection circuit as claimed in claim 1,~~ wherein each diode is a PN junction diode formed by placing a doped area of a first conductivity type in a first well of a second conductivity type, a deep well of the first conductivity type formed under the first well to isolate the first well from a substrate of the second conductivity type.

3. (Original) The ESD protection circuit as claimed in claim 2, wherein the first well is surrounded by a second well of the first conductivity type.

4.-26. (Cancelled)

27. (New) An electrostatic discharge (ESD) protection circuit with low input capacitance, suitable for an I/O pad, comprising:

a first power line;

a second power line; and

a plurality of diodes, stacked and coupled between the first power line and the I/O pad, wherein during normal operation, the diodes are reverse-biased, and, when an ESD event occurs between the second power line and the I/O pad, the diodes are forward-biased to conduct ESD current;

wherein the ESD protection circuit further includes a power-rail ESD clamp circuit, set between the first power line and the second power line, the power-rail ESD clamp circuit being turned on to conduct the ESD current when the ESD event occurs.

28. (New) The ESD protection circuit as claimed in claim 27, wherein the power-rail ESD clamp circuit includes a substrate-triggered MOS of the first conductivity type, the substrate-triggered MOS including two source/drains and a substrate, the two source/drains coupled to the first power line and the second power line respectively, the substrate biased with suitable current to trigger a bipolar junction transistor parasitizing in the substrate-triggered MOS, and conducting ESD current when the ESD event occurs.

29. (New) The ESD protection circuit as claimed in claim 28, wherein the substrate-triggered MOS includes a gate applied with a first bias voltage to keep the substrate-triggered MOS off during normal operations.

30. (New) The ESD protection circuit as claimed in claim 29, wherein the gate is applied with a second bias voltage to speed up the turn-on rate of the substrate-triggered MOS when the ESD event occurs.

31. (New) The ESD protection circuit as claimed in claim 28, wherein the substrate-triggered MOS is formed in a first well of a second conductivity type, a deep well of a first conductivity type being formed under the first well to isolate the first well from a substrate of the second conductivity type.

32. (New) The ESD protection circuit as claimed in claim 31, wherein the first well is surrounded by a second well of the first conductivity type.

33. (New) The ESD protection circuit as claimed in claim 27, wherein the power-rail ESD clamp circuit includes an ESD detection circuit to detect the occurrence of the ESD event.

34. (New) An electrostatic discharge (ESD) protection circuit with low input capacitance, suitable for an I/O pad, comprising:

a first power line;

a second power line; and

a plurality of diodes, stacked and coupled between the first power line and the I/O pad, wherein during normal operation, the diodes are reverse-biased, and, when an ESD event occurs

between the second power line and the I/O pad, the diodes are forward-biased to conduct ESD current;

wherein the diodes include a PN junction diode formed with and between a source/drain of a MOS and a substrate of the MOS.